02-6392/1D

IN THE CLAIMS

1. (canceled)
2. (canceled)
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13. (canceled)
14. (canceled)
15. (canceled)
16. (canceled)
17. (canceled)

18. (currently amended) In an integrated circuit, the improvement comprising a metal interconnect including:

a copper layer formed between dielectric structures, where the dielectric structures have an upper level, where the upper level of the dielectric structures is substantially uniform across all of the dielectric structures,

the copper layer planarized to be ~~no higher than~~ below the upper level of the dielectric structures, the copper layer having no dishing between the dielectric structures, and

an electrically conductive capping layer over all of the copper layer, with none of the capping layer over any of the dielectric structures.

19. (original) The integrated circuit of claim 18, wherein the capping layer is at least partially above the upper level of the dielectric structures.

20. (original) The integrated circuit of claim 18, wherein the electrically conductive capping layer comprises an alloy of at least one of cobalt and nickel.

21. (new) The integrated circuit of claim 18, wherein the copper layer comprises copper formed by electrochemical deposition.

22. (new) The integrated circuit of claim 18, wherein the copper layer is planarized by electrochemical polishing.

23. (new) The integrated circuit of claim 18, wherein the electrically conductive capping layer comprises material formed by electroless deposition.

24. (new) The integrated circuit of claim 18, wherein the dielectric structures comprise low k materials.

25. (new) The integrated circuit of claim 18, further comprising an inter metallic dielectric layer over the electrically conductive capping layer and the dielectric structures.